UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,541	02/10/2004	Amir Morad	13757US03	3126

23446 7590 06/30/2009

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
VO, TUNG T	

ART UNIT	PAPER NUMBER
2621	

MAIL DATE	DELIVERY MODE
06/30/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,541	MORAD ET AL.	
	Examiner	Art Unit	
	Tung Vo	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/10/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 10-20 and 24-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Hinchley (US 6,490,250) as set forth in the previous Office Action dated 10/16/2008.

In the remarks filed on 04/16/2009, the applicant repeatedly argues that Hinchley does not disclose "multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio" pages 9-13.

The examiner respectfully disagrees with the applicant. It is submitted that the multiplexer circuitry of the present invention is disclosed in the specification in figure 5 as follows:

[0040] According to an embodiment of the present invention, device 100 is a parallel digital processor implemented on a single chip and designed for the purposes of real-time video/audio compression and multiplexing, MPEG-1 and MPEG-2 encoding.

[0061] Bitstream processor 112 encodes the compressed video data into a standard MPEG-1 and MPEG-2 format, in accordance with a sequence known in the art of encoding commands. Bitstream processor 112 transfers compressed video data streams to multiplexing processor 114.

[0063] Multiplexing processor 114 multiplexes the encoded video and the encoded audio and/or user data streams (as received from bitstream processor 112 and audio encoder 113) and generates, according to a sequence of optimized multiplexing commands, MPEG-2 standard format streams such as packetized elementary stream, program stream, transport stream and the like. Multiplexing processor 114 transfers the multiplexed video/audio/data streams to a compressed data stream output and to memory controller 110. Multiplexing processor 114 outputs a stream of encoded video and/or audio and/or data.

[0064] Global controller 104 controls and schedules the video input buffer 102, the motion estimation processors 105 and 106, the digital signal processor 108, the memory controller 110, the bitstream processor 112, the 12C/GPIO interface, and the multiplexing processor 114. Global controller 104 is a central control unit that synchronizes and controls all of the internal chip units and communicates with all of the internal chip units using data-instruction-device buses.

The disclosure above encompass the claimed features as “multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a

first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio".

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Let compare the multiplexing circuit of Hinchley and the present invention as follows:

Hinchely

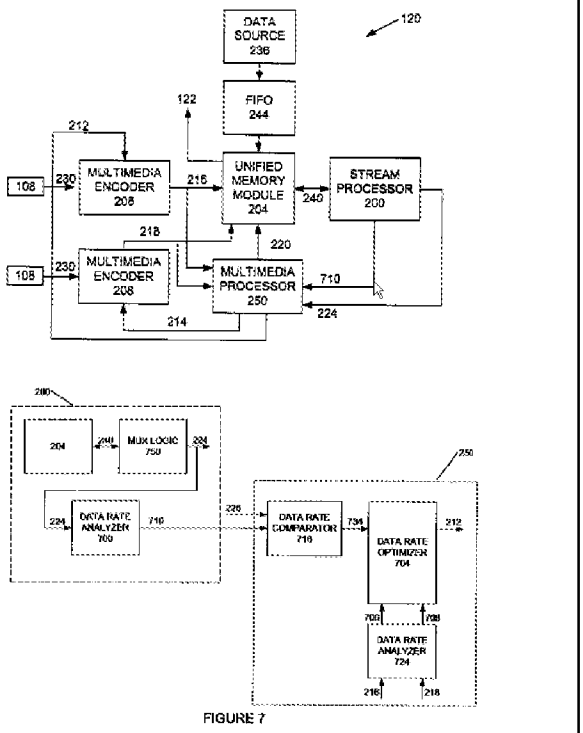
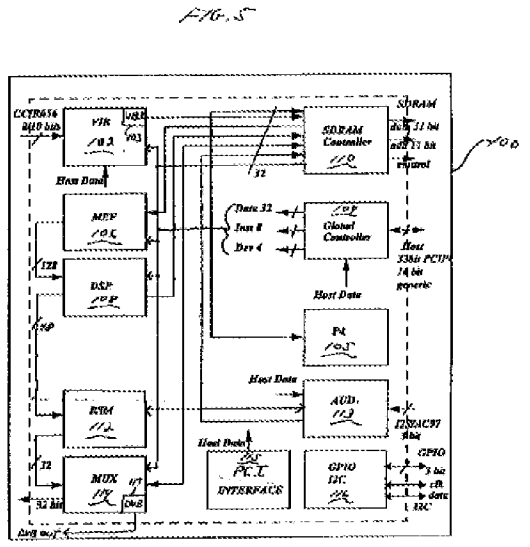


FIGURE 7

FIG. 7 is a more detailed block diagram of an embodiment of the stream processor 200 and multimedia processor 250 in accordance with the present invention. The stream processor 200 includes MUX logic 750 which performs conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined multimedia stream 224. Combined multimedia stream 224 is preferably a program or transport stream as specified in MPEG2. The MUX logic 750 accesses the unified memory module 204 through data line 240 to retrieve the data and the instructions to perform on the data. After performing the required operations, the data 224 is temporarily written back to memory 204, for later transfer to the communications device 112 or other recipient of the Program or Transport Stream 224.

The present invention



[0063] Multiplexing processor 114 multiplexes the encoded video and the encoded audio and/or user data streams (as received from bitstream processor 112 and audio encoder 113) and generates, according to a sequence of optimized multiplexing commands, MPEG-2 standard format streams such as packetized elementary stream, program stream, transport stream and the like. Multiplexing processor 114 transfers the multiplexed video/audio/data streams to a compressed data stream output and to memory controller 110. Multiplexing processor 114 outputs a stream of encoded video and/or audio and/or data.

This disclosure encompasses the claimed features

Based upon the comparison above, Hinchley's MUX logic (750 of fig. 7) has the same functions (MPEG2 standards) as Multiplexing processor (114 of fig. 5) of the present invention. Therefore, Hinchley clearly anticipates the claimed features.

The applicant further argues that Hinchley does not teach "a first encoder" and "a second encoder" as claimed, pages 12-14.

The examiner strongly disagrees with the applicant. It is submitted that Hinchley teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention. Therefore, the functions of MPEG-2 encoders (208 of fig. 2) of Hinchley meet the claimed features.

The applicant further argues that Hinchley fails to teach "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder" as claimed.

The examiner respectfully disagrees with the applicant. It is submitted that Hinchley teaches the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchley et al. (US 6,490,250) in view of Ishihara et al. (US 6,516,031) as set forth in the previous Office Action dated 10/16/2008.

5. Claims 23 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchley et al. (US 6,490,250) in view of Ishihara et al. (US 6,516,031) and further in view of Kopet et al. (US 5,448,310) as set forth in the previous Office Action dated 10/16/2008.

6. Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) as set forth in the previous Office Action dated 10/16/2008.

In the remarks filed on 04/16/2009, the applicant repeatedly argues that the cited portion of Krishnamurthy in the Office Action does not teach " wherein the multiplexer circuitry operates in a first mode that multiplexes the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio to produce a first multiplexed stream coupled via a first output to circuitry external to the device, and operates in a second mode that multiplexes the first compressed video and the first compressed audio to produce the first multiplexed stream coupled via the first output to circuitry external to the device and

multiplexes the second compressed video and the second compressed audio to produce a second multiplexed stream coupled via a second output to circuitry external to the device".

The examiner respectfully disagrees with the applicant. It is submitted that the multiplexer circuitry *(308 of fig. 3, note the stat-mux board can receive up to 24 different channels of transport bit-streams, col. 18, lines 50-52, from 24 encoders,306-306N of fig. 3, N=24, col. 18, line 15)*operates in a first mode *(col. 20, lines 22-26, "a multi-channel mode" would obviously be considered as a first mode, and the first mode is controlled by the overall board-level controls, col. 19, lines 39-42)* that multiplexes the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio to produce a first multiplexed stream *(Note the stat-mux, 308 of fig. 3, multiplexes up to 24 different channels of the transport bitstreams from 24 encoders, therefore the stat-mux would encompass to multiplex the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio as four different channels of transports of bitstreams)* coupled via a first output to circuitry external to the device *(Note the output of the stat-mux, 308 of fig. 3, would be transmitted to circuitry external to the device, 506, 510, 330 of fig. 5; col.19, lines 50-52; the on-chip DMA will automatically move data from the TS output buffer of on-chip memory to the serial output port, this is evidence that the multiplexed compressed bitstreams are transmitted to the serial output port as circuitry),* and operates in a second mode that multiplexes the first compressed video and the first compressed audio to produce the first multiplexed stream coupled via the first output *(Note the stat-mux, 308 of fig. 3, can receives up to 24 different channels of transport bitstreams from 24 encoders; this would fairly suggest, one skill in the art to use the stat-mux, 308 of fig. 3, to multiplex the first compressed video and the*

first compressed audio to produce the first multiplexed stream; col. 19, lines 42-45, 328 of fig. 3, SSI of fig. 3) and multiplexes the second compressed video and the second compressed audio to produce a second multiplexed stream coupled via a second output (*Note the stat-mux, 308 of fig. 3, can receives up to 24 different channels of transport bitstreams from 24 encoders, this would fairly suggest, one skill in the art to use the stat-mux, 308 of fig. 3, to multiplex the second compressed video and the second compressed audio to produce the first multiplexed stream; col. 19, lines 42-45, 328 of fig. 3, SSI of fig. 3);* and the first and second multiplexed outputs are transmitted to circuitry external to the device *(342 of fig. 3, see also 506 and 510 of fig. 5, the stat-mux, 308 of fig. 5, transmits the multiplexed outputs to circuitry external to the device; col.19, lines 50-52, the on-chip DMA will automatically move data from the TS output buffer of on-chip memory to the serial output port, this is evidence that the multiplexed compressed bitstreams are transmitted to the serial output port as circuitry).*

Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, or harmonize all operations of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuits properly working. Since Krishnamurthy teaches the MPEG-2 encoder chip that would obviously has a control function to synchronize the multiplexer, audio and video encoders according the MPEG-2 standards, therefore one of ordinary skill in the art to modify the control function according to MPEG-2 into the CPU (304 of fig. 3) to perform synchronization. In view of the discussion above, the claimed features are unpatentable over Krishnamurthy.

In response to applicant's argument of the obviousness, the examiner would like point out the following basic principle of a proper prior art analysis within 35 U.S.C. 103 (a).

Not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. In re Preda, 401 F.2d 825, 159 USPQ 342 (CCPA 1968) and In re Shepard, 319 F.2d 194, 138 USPQ 148 (CCPA 1963). Skill in the art is presumed. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985). Furthermore, artisans must be presumed to know something about the art apart from what the references disclose. In re Jacoby, 309 F.2d 513, 135 USPQ 317 (CCPA 1962).

The obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969)). Every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein. In re Bode, 550 F.2d 656, 193 USPQ 12 (CCPA 1977).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Office Action above, paragraph 9, suggests all limitations to make obvious the claimed invention.

7. Claims 13 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Bruck (US 6,519,289) as set forth in the previous Office Action dated 10/16/2008.

8. Claims 14, 17-19, 27, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Hinchley et al. (US 6,490,250) as set forth in the previous Office Action dated 10/16/2008.

9. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Boice et al. (US 6,823,013) as set forth in the previous Office Action dated 10/16/2008.

10. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Boice et al. (US 6,823,013) further in view of further in view of Kopet et al. (US 5,448,310) as set forth in the previous Office Action dated 10/16/2008.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung Vo whose telephone number is 571-272-7340. The examiner can normally be reached on Monday-Wednesday, Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tung Vo/
Primary Examiner, Art Unit 2621